# Ken Hunt

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## OVERVIEW

Highly experienced technical engineering manager/director with an excellent track record of managing and developing team members.

Experienced in developing custom IP for large blue chip international companies and with reporting to local and remote line managers.

## SPECIFIC SKILLS and ABILITIES

- Excellent communication and interpersonal skills.
- Experienced in liaising with remote engineering and management organizations.
- Pragmatic approach to every day work challenges and capable of making strategic decisions with little guidance.
- Strong lateral thinking skills with a proven ability to solve technical issues when confronted with design, software or hardware problems.
- Deep understanding of CMOS mixed signal design techniques and of off chip challenges (supply/signal integrity issues, power management, interfacing, test, PCB, discrete components etc).
- Good appreciation of ASIC/ASSP challenges (Timing closure, place and route, ESD, DFM, yield etc)
- Capable of providing accurate project resource and duration estimates and working to critical project deadlines to deliver quality designs on time.
- Adept at working and interfacing with internal and external customers in a professional manner.
- Good track record of interviewing and recruiting the right people for specialist roles (including graduates, technicians, engineers and managers).
- Extensive tool and operating systems experience: Schematic capture (Cadence entry), Simulation (Verilog, Hspice, Hsim, Xa, Nanosim etc), full custom layout (Cadence) and verification, Logic modeling and verification (Verilog, Synopsys, Vtran), documentation (Word/Framemaker), Programming and scripting. Windows/Microsoft Office, Linux administration etc.

## INDUSTRIAL EXPERIENCE

### 2017-Present Director Analog – Socionext Europe GmbH

Responsible for directing various high speed data converter development teams in the UK and Germany ranging from 4G/5G wireless converters through to high speed (140Gsps) optical transport converters. Main responsibilities include:-

- Technical marketing of existing products and new products under development.

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- Representing Socionext (Networking Division) at trade shows such as ECOC (European Conference on Optical Communication) and OFC (Optical Fiber Conference).
- Providing ongoing customer support and ensuring customers are kept informed of development progress.
- Helping the Network business unit define the future product roadmap.
- Directing development teams to deliver against roadmap.
- Ensuring design innovation and quality within the development teams is kept to a very high standard.
- Managing development costs and managing, developing and appraising staff.

**2013-2016 Senior Custom IP Design Manager - Micron Europe ltd**

Responsible for managing a design team developing a highly complex, high speed TSV (through silicon via) memory interface used within Micron's HMC (Hybrid Memory Cube) product offering. The design uses state of the art 14nm Finfet technology and has extremely tight timing requirements. Main responsibilities include:-

- Ensuring all internal IP developed is of good quality.
- Overseeing all IP design, signal integrity work and power analysis efforts.
- Ensuring tools and flows (PDK setups, design capture, simulation, modeling etc.) is of a suitable standard.
- Writing and ensuring team and development work is ISO9001 compliant.
- Managing, developing and appraising staff.

**2009–2013 Senior IP Design Manager - Aptina (UK) ltd (formerly Micron Europe ltd)**

Responsible for managing an engineering team tasked with developing all of the library IP used within Aptina, managing the development of sensor specific analogue IP and for managing the Laboratory services in Bracknell. Main responsibilities included:-

- Overseeing the development of IOs, high speed SerDes PHYs, memories, PLLs and periphery circuitry across multiple technology nodes.
- Ensuring right first time and on time IP development.
- Overseeing the laboratory staff to ensure all IP and products were fully verified.
- Developing future strategies and company IP direction/definitions.
- Managing, developing and appraising staff.

**2002–2008 Chief Engineer - Aptina (UK) ltd (formerly Micron Europe ltd)**

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Acted as mentor to others and had responsibility for being a technical authority on IP development and direction within Aptina/Micron UK. As part of the strategic IP development role personal responsibilities included:-

- Attending customer.
- The design and development of the worlds first MIPI DPHY transmitter. This design is still in use today and is often used as a reference platform by other companies for validating their DPHY receivers.
- The development of Aptina's proprietary HiSPi (Hi SPeed Interface) used in many camera platforms. HiSPi is a scalable, synchronous, low power serial data bus and protocol which is rapidly becoming Aptina's default interface and has been successfully demonstrated with a large format imaging sensor which had 30 serial data lanes running @ 700Mbps.
- The architecture, design and realisation of a serial, high speed 'Stereo' (3D) imager interface capable of keeping 2 image sensors in complete pixel alignment.

**1998-2002 Circuit IP design Manager - Micron Europe ltd (formerly Rendition UK ltd)**

Interviewed and employed by Rendition which was later absorbed into Micron. Following on from the closure of the UK design organization at LSI, joined Rendition as an established manager with 15 other LSI team members reporting to me. Responsibilities included:-

- Establishing an IP development capability using Micron's own (dram) process targeting eDram applications.
- Making tool choices and design flow decisions along with specifying and guiding the development of an in-house characterisation tool.

**1995-1998 Senior Circuit Design Manager - LSI Logic Europe plc**

Promoted to Senior Manager in 1995 as a result of the groups success and increased profile within the company. At the same time LSI adopted a global engineering strategy. The design work remained similar although working practices changed dramatically. Role included:-

- Responsibility for all the Corporate Products Division staff in Bracknell. Reporting directly to the VP of Corporate Products (US based).
- Introducing a Memory development capability in Europe to support additional memory development requests.
- Increasing the scope of development activities to include larger development projects (Flash Analogue-to-Digital Converters, Memory compilers etc.).
- Appointing managers as the group grew. (the group was divided into two sections: Mixed Signal and Memory Development).

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- Taking on responsibility of HyperPHY project (Very high speed PHYs) and a small Characterisation team.

**1992–1995 Circuit Design Manager - Lsi Logic Europe plc**

Hired by LSI to help establish a custom ASIC IP design capability. Achievements included**:-**

- Establishing a CMOS Custom Cell Development flow in Europe.
- Demonstrating a working flow by developing the first custom CMOS cell for LSI Logic Europe.
- Promoting Custom Cell development capability throughout Europe to different design centres and to key customers.
- Forming a design group to support the increasing European business opportunities.
- Later formalising the design flow for ISO9000 certification.
- Managing budgets for pay, software purchase, software maintenance and contractors.
- Developing many Mixed Signal functions including Phase Locked Loops, Delay Locked Loops, Crystal Oscillators, Clock and Data Recovery blocks as well as High Speed (> 1Gbit/s) LVDS, PECL and PCML IO's.

**1988–1992 Tactical Cell Design Group Manager - Texas Instruments Bedford**

Promoted to Manager of the Tactical Cell Group and took on responsibility of 5 staff.

- Responsible for all of the Tactical Cell Group promotion, development and support work in Europe.

**1986–1988 Analogue Design Engineer - Texas Instrument Bedford**

Joined TI as an Analogue Design Engineer in the ASIC Design Centre (Bedford) developing "Tactical" cells.

**EDUCATION**

**1983-1986 University of Brighton (formerly Brighton Polytechnic).**

Bsc (hons) Degree in Electronic Engineering (Upper 2nd Class).

**1976-1983 Tunbridge Wells Grammar School for Boys**

'A' Levels: Mathematics, Physics, Electronics, Engineering Drawing & Engineering.

'O' Levels: Mathematics, Engineering drawing, Engineering, Physics & Chemistry.

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## INTERESTS

**Science/Engineering:** General interest and fascination for technology. Including experimenting with Microprocessors, remote control applications, robotics, audio (amplifiers - class D especially), automotive electronics, computer control/mechatronics and general mechanics.

## PATENTS

I have ~20 patents to my name.